Real-Time Evaluation of Control Strategies Using a Hybrid Hardware-in-the-Loop (H-HIL) Framework

Tanmay Wankhade[1], Shubh Arekar[2], Madhumita Patil[3], Sunny Kumar[4]

***Abstract*— This paper presents a Hybrid Hardware-in-the-Loop (H-HIL) framework that bridges the gap between SIL simulations and full HIL configurations. By integrating a Typhoon HIL 602+ real-time simulator with a dSPACE DS1104 controller via analog I/O interfacing, the framework achieves a unique balance between computational flexibility and hardware realism. The framework is validated on a modified IEEE 9-bus microgrid with renewable integration. The results show that analog delay and noise introduce hardware-dependent transient behaviors: deeper frequency dip, voltage overshoot, and post-fault oscillations that pure SIL cannot predict. In addition, the flexible structure of the framework allows standalone components to be added between the emulated plant and controller domains, enabling rapid prototyping of subsystems under realistic operating conditions.**

Keywords— Hybrid Hardware-in-the-Loop, Typhoon HIL, dSPACE, microgrid, real-time simulation, control validation

I. Introduction

The growing use of renewable energy systems makes control design and testing more complex and harder to handle with conventional frameworks [1], [2]. While Software-in-the-Loop (SIL) simulations are commonly used for controller prototyping, they often miss analog-domain effects such as measurement latency, sensor noise, and interface delay, all of which can significantly affect closed-loop performance [3], [4]. HIL testing improves testing accuracy by coupling a simulated environment with physical hardware components. Conventional HIL approaches are typically categorized as **Controller-HIL (C-HIL)**, where a real controller interfaces with a simulated plant, and **Plant-HIL (P-HIL)**, where a simulated controller interacts with a physical power plant [5]. Although these methods achieve high experimental accuracy, they require finalized hardware prototypes and complex protection mechanisms, making them harder to use at early stages of design and algorithm-level validation.

To address this gap, a **Hybrid Hardware-in-the-Loop (H-HIL)** framework is proposed that closes the gap between SIL and full HIL in both theory and practice. Fig. 1 shows how the H-HIL concept uses analog I/O interfacing and real-time computation to mimic both the plant and controller domains. This captures key analog characteristics such as delay, phase lag, and noise without requiring the final embedded controllers. The setup supports early-stage, hardware-aware testing by integrating a **Typhoon HIL 602+** real-time simulator and a **dSPACE DS1104** controller board, connected via analog I/O.

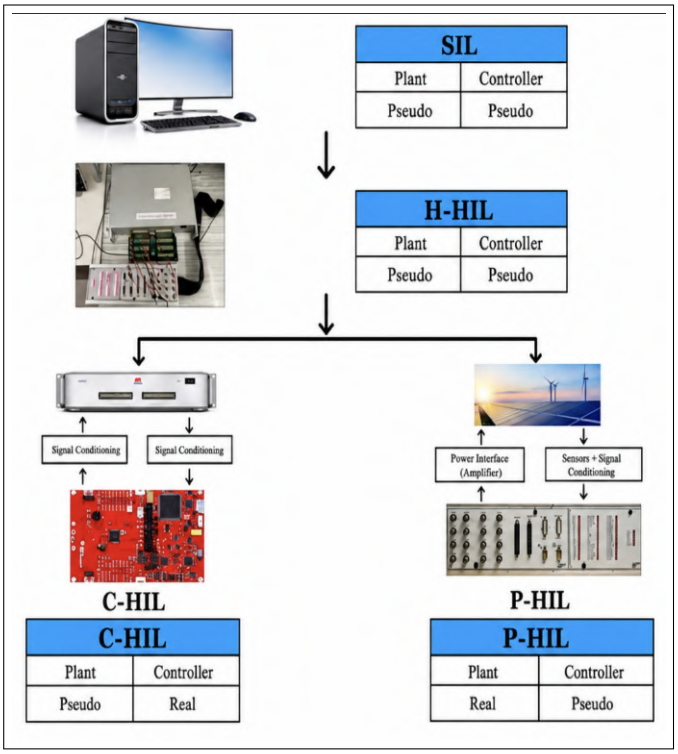

Fig. 1: Conceptual hierarchy of SIL, H-HIL, and traditional HIL frameworks. H-HIL occupies an intermediate position: both the plant and controller are emulated on real hardware platforms and coupled via analog I/O, enabling hardware-realistic interaction without requiring finalized embedded controllers.

Another advantage of the H-HIL setup is its flexibility. Since the plant and controller domains are connected through standard analog I/O interfaces, hardware or software components can be added between them for independent testing. For example, communication modules, signal-conditioning circuits, sensor emulators, cybersecurity layers, fault-detection algorithms, or AI-based decision systems can be tested within the closed-loop environment without needing a finalized physical controller or plant. This makes the H-HIL framework useful beyond just controller testing — it also

*This work was supported by the Electrical-Modeling, Computation, and Control (E-MC^2) Lab, VJTI, Mumbai, India.

[1]Department of Electrical Engineering, VJTI, Mumbai, India. tswankhade_b22@ee.vjti.ac.in

[2]Department of Electrical Engineering, VJTI, Mumbai, India. sparekar_m24@ee.vjti.ac.in

[3]Department of Electrical Engineering, VJTI, Mumbai, India. mspatil_m24@ee.vjti.ac.in

[4]Department of Electrical Engineering, VJTI, Mumbai, India. sskumar@ee.vjti.ac.in

supports component-level checks, integration testing, and early-stage prototyping under realistic real-time conditions.

Fig. 1 shows the classification of SIL, H-HIL, and traditional HIL approaches, highlighting the unique position of H-HIL as a hybrid framework in which both domains are mimicked through real-time analog interfacing. Fig. 2 summarizes how computational complexity, sampling time, and hardware realism change across these testing levels. Prior work from the same lab has demonstrated real-time HIL testbeds for large-scale power system analysis [13]–[15] and FPGA-in-the-loop (FIL) testing of grid-forming inverters [16], building the hardware infrastructure and testing methodology on which the present H-HIL framework is based.

Factors	SIL (Software in Loop)	FIL (FPGA in Loop)	HIL (Hardware in Loop)
Sampling Time (sec)	10^{-3}	10^{-7} - 10^{-8}	10^{-6}
Environment	One environment (one sampling time)	Multiple Pseudo environments (more than one Ts)	Combination of real and pseudo enviroments
Output	Based on Mathematical modelling	Based on Mathematical modelling	Combination of Actual Real component and mathematical model
Component Delay (Per Gate)	9 nanosecond	1 nanosecond	1 microsecond
Architecture constrain	All cores are utilised (no specific cores assigned)	Custom user-defined with fixed logic blocks (LUTs)	Fixed hardware architecture with real time cores (FPGA+DSP)
Computation Burden	High	Low	Moderate
Flexiblity	High (non-real time)	Low (but very efficient)	Moderate
Delay	Delays due to CPU scheduling or OS overhead	Minimal delay but high synthesis complexity	Real Time operation may require model simplification or partitioning

Fig. 2: Comparison of SIL, FIL, and HIL validation frameworks, illustrating trade-offs between flexibility, computational delay, and real-time hardware realism.

II. Real-Time Simulation Configuration

This section describes the hardware setup of the testbed, designed to test power system dynamics and control strategies in a closed-loop framework. The setup uses the Typhoon HIL 602+ and dSPACE DS1104 platforms, with each platform serving a distinct role in simulating and controlling the microgrid, as shown in Fig. 3. The subsections below describe what each platform does, how signals are exchanged between them, and how the two work together to closely match the behavior of a real-world power system.

A. Typhoon HIL 602+ Configuration

The Typhoon HIL 602+ is used to simulate the microgrid power network: the standard IEEE 9-bus model is set up with two synchronous generators replaced by an equivalent photovoltaic (PV) array and a wind turbine to represent a renewable-rich scenario. The model includes transmission

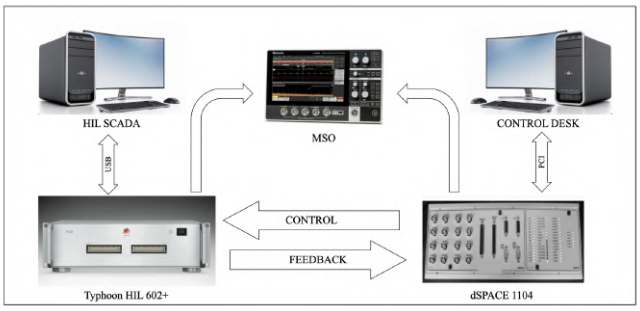

Fig. 3: Real-time testbed interconnection between Typhoon HIL 602+ and dSPACE DS1104.

lines, loads, and power electronic inverters, and runs in real time on FPGA-based hardware that solves circuit equations at high speed. The simulator gives real-time readings of bus voltages, line currents, and active/reactive power flows and, because no physical power hardware is needed, it allows safe testing of rapid load changes and fault conditions. This high-accuracy real-time environment is therefore a good fit for testing control strategies under realistic grid dynamics [3], [6].

Real-time signals (voltages, currents, and power flows) are sent from the Typhoon HIL simulator to the dSPACE DS1104 controller via analog I/O to create a closed-loop testbed where control actions are updated based on measured feedback. The measured end-to-end delay in a typical setup was 20 ms, calculated via dSPACE timestamps; however, dSPACE execution time can increase as controller complexity or signal path length grows. A 20 ms delay is significant for fast loops such as phase-locked loops (PLLs) or primary droop control, as it reduces phase margin and can cause delayed responses, increased overshoot, oscillations, or even instability. As a result, delay-aware tuning, compensation (e.g., predictive or feedforward elements), or faster I/O processing chains should be considered when testing high-bandwidth control loops in the H-HIL environment.

B. dSPACE DS1104 Configuration

The microgrid's master controller runs on the dSPACE DS1104 real-time board using C code and a standard PI controller. Its main job is to control the active and reactive power output of Distributed Energy Resources (DERs) to maintain voltage and frequency stability in both grid-connected and islanded modes. In islanded mode, one DER (e.g., a battery inverter) operates in grid-forming mode while the others follow the grid. The controller continuously receives measurements from the grid model running on Typhoon HIL 602+ including power output ($P_{\text{PCC}}, Q_{\text{PCC}}$) and grid frequency and computes updated target values for each DER [3].

Frequency and voltage regulation is performed using classical droop control equations [8]:

$$\omega_{\text{ref}} = \omega_{\text{nom}} + \Delta\omega_{\text{off}} - K_P(P_{\text{meas}} - P_{\text{ref}}) \quad (1)$$

$$V_{\text{ref}} = V_{\text{nom}} + \Delta V_{\text{off}} - K_Q(Q_{\text{meas}} - Q_{\text{ref}}) \quad (2)$$

where K_P and K_Q are the frequency and voltage droop coefficients, respectively, and the offset terms $\Delta\omega_{\text{off}}$ and ΔV_{off} are used for secondary control adjustment. A power-balancing PI controller is layered on top of this to drive P_{PCC} and Q_{PCC} toward zero by computing correction signals:

$$P_{\text{off}}(t) = K_{pP}(-P_{\text{PCC}}) + K_{iP}\int_0^t (-P_{\text{PCC}})\,d\tau \tag{3}$$

$$Q_{\text{off}}(t) = K_{pQ}(-Q_{\text{PCC}}) + K_{iQ}\int_0^t (-Q_{\text{PCC}})\,d\tau \tag{4}$$

It is worth noting that the droop controller includes a secondary (integral) control layer via the PI correction terms P_{off} and Q_{off} which brings the steady-state frequency back to 60 Hz after a load step. The primary droop action causes a short-lived frequency drop proportional to the load change; the integral layer then removes this steady-state error. As a result, the frequency fully recovers to 60 Hz after the 10% load step in Fig. 6, which is the expected behavior of the two-level control structure used here.

With this approach, DER target values react to grid disturbances in real time. In grid-connected mode, the controller tracks power flow without actively regulating; after islanding, it adjusts P_{ref} and Q_{ref} using the computed offsets to stabilize the system and maintain power balance.

C. Alternative Grid-Forming Control Strategies

Beyond droop-based control, other grid-forming (GFM) strategies such as Virtual Synchronous Machine (VSM) control and Dispatchable Virtual Oscillator Control (dVOC) can also be used within the H-HIL framework [11], [12].

1) Virtual Synchronous Machine (VSM): VSM control copies the behavior of a synchronous generator by adding virtual inertia and damping, which improves frequency stability during disturbances. The governing equations are:

$$M\dot{\omega} = (P^* - P) - D(\omega - \omega_0) \tag{5}$$

$$V^* = V_0 - n_q(Q - Q^*) \tag{6}$$

where $M = \frac{2HS_{\text{nom}}}{\omega_0}$ is the virtual inertia, H is the inertia constant, S_{nom} is the rated apparent power, D is the damping constant, and m_p, n_q are droop coefficients.

2) Dispatchable Virtual Oscillator Control (dVOC): dVOC is inspired by nonlinear oscillator synchronization, programming inverters to behave as weakly nonlinear oscillators. It synchronizes rapidly without PLLs while reducing to droop-like behavior in steady state. The dynamics are:

$$\dot{V}^* = \mu\big(V_0^2 - (V^*)^2\big)V^* - \frac{2\eta}{3V^*}(Q - Q^*) \tag{7}$$

$$\dot{\theta} = \omega = \omega_0 - \frac{2\eta}{3(V^*)^2}(P - P^*) \tag{8}$$

where μ and η are design parameters controlling the amplitude restoration speed and the power-angle coupling strength, respectively.

D. Interconnected H-HIL Configuration

The core of this testbed is the interconnection through which signals are exchanged and real-world imperfections are introduced, making the simulation more realistic. Analog output channels send power measurements from the Typhoon HIL simulation to the dSPACE DS1104 analog inputs. The dSPACE board digitizes these measurements internally, which the control algorithm then uses to compute new reference commands. The updated active and reactive power target values ($P_{\text{ref}}, Q_{\text{ref}}$) are then sent back to the Typhoon HIL analog inputs via dSPACE analog outputs. This closed-loop setup ensures that Typhoon HIL receives control signals just as they would be generated by a real controller, allowing hardware-aware testing of microgrid control strategies under realistic conditions [9].

The limitations of the proposed setup include: (i) scaling to larger networks is limited by the number of available analog I/O channels; (ii) the analog interface introduces a fixed delay that may not match all physical hardware; and (iii) purchasing both Typhoon HIL 602+ and dSPACE DS1104 platforms costs more than pure SIL, though it is still much cheaper than full C-HIL or P-HIL setups.

III. Validation Methods

A baseline is first set up using a Typhoon-only real-time simulation mode, referred to as *real-time Software-in-the-Loop (RT-SIL)*. In this setup, the Typhoon HIL 602+ platform runs the modified IEEE 9-bus microgrid model on its own, with PV and wind turbine units replacing two traditional synchronous generators, the master controller running entirely in software, and no analog I/O interface in use.

Two categories of benchmark tests are performed:

1) **Step-Load:** Step changes of $+10\%$ are introduced in both active (P) and reactive (Q) power demand to evaluate the controller's capability to maintain frequency and voltage regulation.
2) **Fault:** A line-to-line (L-L) fault is applied between buses 4 and 5 for a duration of 0.5 s to assess dynamic response and fault-clearing performance.

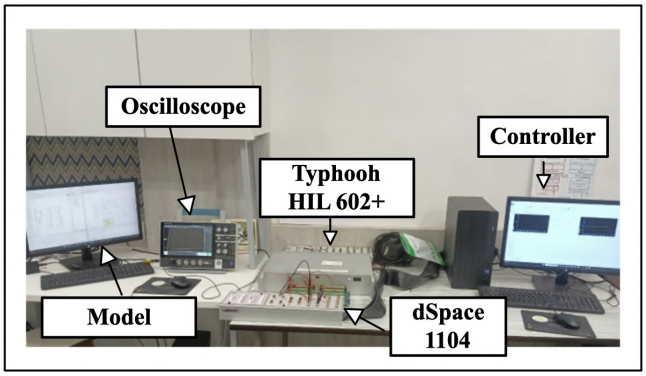

Fig. 4: Experimental setup in the $E\text{-}MC^2$ Lab used for validating microgrid control performance in real time.

Note on data resolution: The simulation data exported from Typhoon HIL and dSPACE was logged at 0.5 s intervals due to storage constraints during real-time execution. While this resolution is sufficient to observe the primary transient events (frequency minimums, voltage dip, and post-fault recovery), finer transient dynamics such as sub-cycle oscillations are not fully resolved in the presented waveforms. Future experiments will employ higher-frequency logging to capture sub-second transient behavior more completely.

IV. Results and Discussion

The modified IEEE 9-bus microgrid model used in the experiments is depicted in Fig. 5, with PV and wind sources replacing two traditional synchronous generators. Under two test scenarios (1) a 10% step increase in active/reactive power (PQ load) and (2) a line-to-line (L–L) fault the controller is evaluated for its ability to maintain a nominal frequency of 60.0 Hz and a per-unit voltage of 1.0 pu at the point of common coupling (PCC).

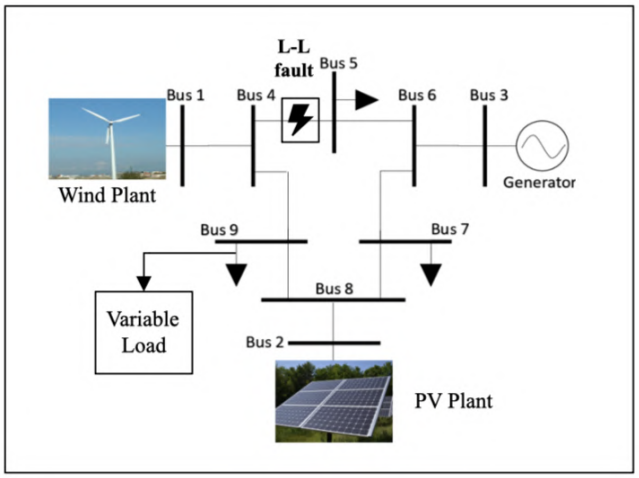

Fig. 5: Modified IEEE 9-bus microgrid model used in SIL and H-HIL simulations, with PV and wind sources replacing two synchronous generators.

A. Variable PQ Load

Load changes put the system under pressure and test the controller's dynamic response. At $t = 20$ s, active power demand increases by 10%. Fig. 6 shows that both SIL and H-HIL show a frequency dip; however, H-HIL (red) shows a deeper dip and slower recovery than SIL (blue), due to analog signal delays in the control loop. The added delay mimics the real-world delay from measurement, computation, and actuation. As described in Section II-B, the two-level droop-plus-PI controller includes secondary integral action that restores the steady-state frequency to 60 Hz; the deeper H-HIL dip reflects the delayed fault detection introduced by the analog interface.

At $t = 46$ s, reactive power demand increases by 10%. As shown in Fig. 7, both systems experience a voltage dip to approximately 0.94 pu. SIL recovers smoothly to 0.98 pu.

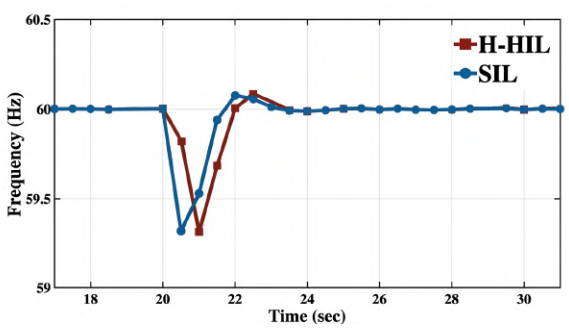

Fig. 6: Frequency response for a 10% step increase in active power load at $t = 20$ s.

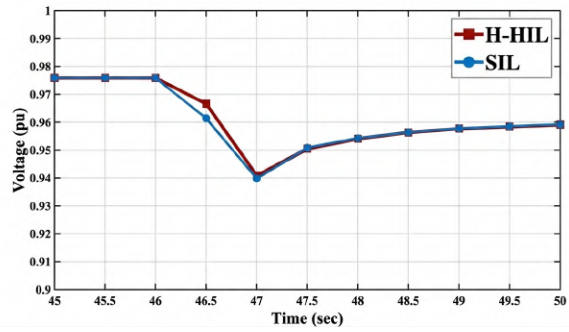

Fig. 7: Voltage response for a 10% step increase in reactive power load at $t = 46$ s.

B. Line-to-Line (L–L) Fault

A line-to-line (L–L) fault is introduced between buses 4 and 5 at $t = 26$ s and cleared at $t = 26.5$ s. Fig. 8 shows that both setups experience a frequency dip. SIL bottoms out near 58.5 Hz, while H-HIL dips to approximately 55.0 Hz and shows stronger oscillations due to delayed fault detection and analog-induced phase lag.

Fig. 9 shows voltage recovery after fault clearance. SIL returns to nominal voltage with minimal overshoot. H-HIL, however, overshoots above 1.3 pu before settling, caused by delayed fault-clearance recognition in the analog interface. The 1.3 pu overshoot seen in H-HIL is an artifact of the analog interface delay rather than a physical instability; in a real deployment, protective relay thresholds would need to account for such short-lived voltage spikes introduced by measurement and actuation delays.

Fig. 10 summarizes the experimentally measured SIL and H-HIL performance metrics under both load and fault conditions.

V. Conclusion

This paper presented an H-HIL framework that closes the gap between SIL simulations and full HIL configurations. By integrating a Typhoon HIL 602+ real-time simulator with a dSPACE DS1104 controller through analog I/O interfacing, the framework achieves a good balance between computational flexibility and hardware realism.

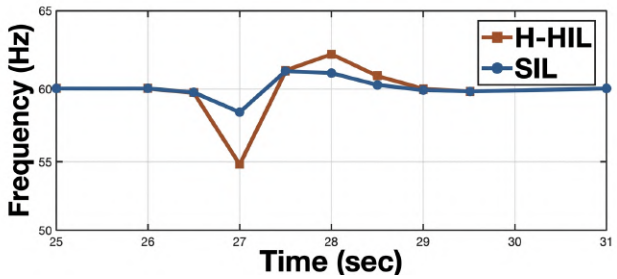

Fig. 8: Frequency response during a line-to-line fault between buses 4–5 ($t = 26$–26.5 s).

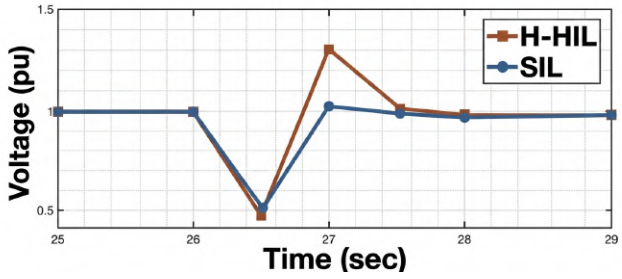

Fig. 9: Voltage recovery following line-to-line fault clearance.

The key contributions are: (1) a formal definition of H-HIL as an intermediate testing level; (2) a working testbed combining Typhoon HIL 602+ and dSPACE DS1104 via analog I/O; and (3) measured proof that analog delay and noise introduce hardware-dependent transient behaviors: deeper frequency dip, voltage overshoot, and post-fault oscillations that pure SIL cannot predict.

In addition, the flexible structure of the H-HIL framework allows standalone components to be added between the emulated plant and controller domains. As a result, individual modules such as communication interfaces, protection relays, estimation algorithms, AI agents, or embedded devices can be tested independently without needing the complete controller or the full physical plant. This lets developers check subsystem functionality, interface compatibility, and real-time performance at an early stage of development, which reduces integration risks and speeds up system deployment.

These results show that H-HIL is a practical middle-ground testing step, giving engineers a controlled setting to find hardware-dependent issues before building physical prototypes. The framework is hardware-aware, software-flexible, and affordable, making it suitable for both research and teaching in power electronics and microgrid labs. Future work will include communication-delay simulation, experimental testing of the VSM and dVOC strategies presented in Section II-C, and higher-resolution data logging to capture sub-second transient behavior. Beyond microgrids, the H-HIL approach has potential as a single testing framework for embedded control systems in other application areas.

Test Scenario	Observed Quantity	SIL	H-HIL	Key Observation
10 % Active-load step (t = 20 s)	Frequency nadir (Hz)	59.3	59.3	Both reach the same nadir; H-HIL requires ≈ 0.3–0.5 s longer to stabilize due to analog-loop latency.
	Recovery duration (s)	≈ 1.8	≈ 2.3	H-HIL shows slower damping caused by phase lag and interfacing delay.
10 % Reactive-load step (t = 46 s)	Minimum voltage (pu)	0.96	0.96	Nearly identical dip, confirming consistent controller response.
	Frequency nadir (Hz)	58.5	55.0	H-HIL exhibits a deeper transient dip (≈ −6 %) due to delayed fault detection and analog-phase lag.
Line-to-Line fault (t = 26–26.5 s)	Voltage overshoot (pu)	1.10	1.30	Overshoot in H-HIL (≈ +18 %) arises from over-correction during delayed fault clearance.
	Post-fault recovery trend	Stable < 0.8 s	Stable ≈ 1.0 s	Both recover without instability; H-HIL shows longer restoration.

Fig. 10: Summary of experimentally measured SIL and H-HIL performance under load step and fault conditions.

ACKNOWLEDGMENT

The authors are grateful for the research guidance of Prof. Alex Stankovic, Prof. N. M. Singh, and Dr. S. R. Wagh. The authors also acknowledge the support of the Electrical-Modeling, Computation, and Control (E-MC^2) Lab, VJTI, Mumbai, India.

REFERENCES

[1] D. E. Olivares, A. Mehrizi-Sani, A. H. Etemadi, C. A. Cañizares, R. Iravani, M. Kazerani, A. H. Hajimiragha, O. Gomis-Bellmunt, M. Saeedifard, R. Palma-Behnke, G. A. Jiménez-Estévez, and N. D. Hatziargyriou, "Trends in Microgrid Control," *IEEE Trans. Smart Grid*, vol. 5, no. 4, pp. 1905–1919, Jul. 2014.

[2] S. Ahmad, M. Shafiullah, C. B. Ahmed, and M. Alowaifeer, "A Review of Microgrid Energy Management and Control Strategies," *IEEE Access*, vol. 11, pp. 430–452, 2023.

[3] F. Mihalič, M. Truntič, and A. Hren, "Hardware-in-the-Loop Simulations: A Historical Overview of Engineering Challenges," *Electronics*, vol. 11, no. 15, art. no. 2462, 2022.

[4] E. Limpaecher, R. Salcedo, E. Corbett, S. Manson, B. Nayak, and W. Allen, "Lessons Learned from Hardware-in-the-Loop Testing of Microgrid Control Systems," in *Proc. CIGRE Grid of the Future Symposium*, Cleveland, OH, USA, Oct. 22–25, 2017.

[5] G. Lauss, M. O. Faruque, K. Schoder, C. Dufour, A. Viehweider, and J. Langston, "Characteristics and Design of Power Hardware-in-the-Loop Simulations for Electrical Power Systems," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 406–417, Jan. 2016.

[6] A. Villálon, C. Muñoz, J. Muñoz, and M. Rivera, "A Detailed dSPACE-Based Implementation of Modulated Model Predictive Control for AC Microgrids," *Sensors*, vol. 23, no. 14, art. no. 6288, 2023.

[7] R. O. Salcedo, J. K. Nowocin, C. L. Smith, R. P. Rekha, E. G. Corbett, E. R. Limpaecher, and J. M. LaPenta, "Development of a Real-Time Hardware-in-the-Loop Power Systems Simulation Platform to Evaluate Commercial Microgrid Controllers," MIT Lincoln Laboratory, Lexington, MA, USA, Tech. Rep. TR-1203, Feb. 2016.

[8] D. Chatterjee, J. Triemstra, C. Macías, W. Cai, K. Tatkare, R. Mallik, and B. Johnson, "UNIFI's Grid-Forming (GFM) Inverter Reference Design: A Tutorial on Modeling, Control, and Experimental Implementation of GFM Inverters," National Renewable Energy Laboratory, Golden, CO, USA, Tech. Rep. NREL/TP-5D00-92994, Jul. 2025.

[9] G. Lauss, F. Lehfuss, A. Viehweider, and T. Strasser, "Power Hardware in the Loop Simulation with Feedback Current Filtering for Electric Systems," in *Proc. 37th Annual Conf. IEEE Ind. Electron. Soc. (IECON)*, Melbourne, VIC, Australia, 2011, pp. 3725–3730.

[10] H. Qunhai, K. Li, P. Wei, H. Shengli, and Z. Jing, "The Grid-Connected PV Inverter Control Basing the Exponential Sliding Mode," in *Proc. ISES World Congress 2007 (Solar Energy and Human Settlement)*, Springer, Berlin, Heidelberg, Germany, 2008, pp. 2743–2747.

[11] R. Teodorescu, M. Liserre, and P. Rodríguez, *Grid Converters for Photovoltaic and Wind Power Systems*. Chichester, U.K.: Wiley–IEEE Press, 2011.

[12] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodríguez, "Control of Power Converters in AC Microgrids," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4734–4749, Nov. 2012.

[13] S. Kumar, A. Chavekar, A. Pandey, P. Goswami, and F. Kazi, "Real-Time Hardware-in-Loop Testbed for Power System Analysis," in *Proc. 3rd Int. Conf. Power, Control and Computing Technologies (ICPC2T)*, 2024, pp. 1–6.

[14] S. Kumar, A. Pandey, P. Goswami, P. Pentayya, and F. Kazi, "Analysis of Mumbai Grid Failure Restoration on Oct 12, 2020: Challenges and Lessons Learnt," *IEEE Trans. Power Syst.*, vol. 37, no. 6, pp. 4555–4567, 2022.

[15] A. Pandey, S. Kumar, S. Mohire, P. Pentayya, and F. Kazi, "Dynamic Modeling and Cascade Failure Analysis of the Mumbai Grid Incident of October 12, 2020," *IEEE Access*, vol. 10, pp. 43598–43610, 2022.

[16] O. Sonone, A. Chavekar, P. Goyanka, and S. Kumar, "Grid-Forming Inverter Implementation Using Arty A7 100T: A FIL for Microgrid Analysis," in *Proc. IEEE Power & Energy Society General Meeting (PESGM)*, 2025, pp. 1–5.