# Modeling of CNT MOSFET Transistors Enabling Self-Healing and Healing Procedures

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***Abstract*— The paper analyses the modelling of the voltage/current characterization of Carbon Nanotubes (CNTs) based n-channel MOSFET transistors. The model includes the SPICE and the Finite Element Method (FEM) simulations having the goal to highlight the damage effect on the electrical MOSFET variables and to estimate the sensitivity response of the transistor versus the electrical resistances modelling CNTs damages. The model is able to characterize the single CNT in an n-channel MOSFET layout configuration and the macroscopic effect of damaged multiple CNTs. The performed analysis is suitable to understand the possible control of external stimuli for a self-healing or healing process of the damaged CNTs-based transistor. The paper is concluded by discussing a new measurement TC34 protocol for nanostructured MOSFET healing process procedure.**

## I. Introduction

Carbon Nanotubes (CNTs) are suitable for the implementation of Field Effect Transistors (FETs) implementing gas sensors [1]-[3], detectors of substances [4], pressure sensors [5], pH sensors [6], and bio-sensors [7],[8]. An emergent research issue is the healing (adding new material) and the self-healing/self-repair (auto-healing capacity of the material by applying external stimuli) of nanomaterials [9]-[11]. Specifically, the self-healing of carbon-based materials and CNT-based transistors can be performed by thermal annealing processes [12],[13], conventional resistive heating processes [14], by means the electro-thermal effect [15], or by the self-growth process through spray deposition techniques [16]. By focusing the attention on CNT-based transistors, it is important to estimate the damage effect of CNTs in order to control external stimuli enabling the self-healing and healing of processes. The modelling of CNT Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) [17]-[25] is the first step to understand the degradation effect due to possible damages of CNTs. Furthermore, the new frontiers of research about CNT requires new standards of measurement approaches of the healing and the self-healing process. In this direction, the Technical Committee (TC) number 34 (Nanotechnology in Instrumentation and Measurement) is working to define measurement protocols about self-repairing nanomaterials and devices based on nanostructures thus supporting the study and the standardization of the transistor degradation and of the I-V characterization before and after the recovery process. The state of the art is weak about the CNTs damage characterization. For this purpose, the proposed study is a preliminary theoretical study able to define a basic approach characterizing the electrical behavior of damaged CNTs generating an interruption of the electrical current.

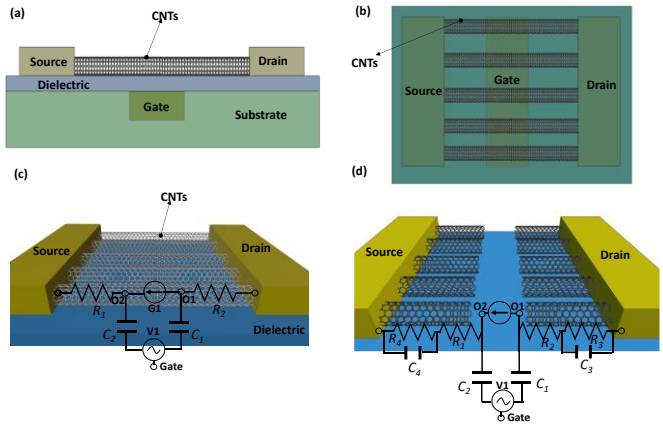


Figure 1. CNT-MOSFET model: (a) front view model; (b) top view model; (c) perspecive and circuit modeling of a single CNT in a MOSFET layout; (d) perspecive and circuit modeling of a single damaged CNT (damaged/interrupted CNT) in a MOSFET layout.

Following the topics listed in this section, the paper will discuss:

- a small signal model (slow variation circuit model) of a single CNT damaged conductive link interconnecting source and drain electrodes of an n-channel MOSFET simulating the resistive effect due to the damage and the related sensitivity response of the voltage signals;

- a circuit model (macroscopic model) simulating the resistive effect of the whole n-type MOSFET damaged transistor calculating its sensitivity response;

- a theoretical Finite Element Method (FEM) model describing the physical effect of the interruptions of the CNTs in the ideal case of aligned CNTs;

- a basic guideline to characterize a measurement protocol of self-healing process of a nanostructured based transistor by measuring I-V characteristics.

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## II. MODELLING

### A. CNT MOSFET transistor layout and circuit model

Following the importance of the topic analyzed in state of the art, the work provides a detailed model simulating the CNTs damage effect about the degradation of the electrical signals by considering an n-channel MOSFET layout of Fig. 1 (a) and Fig. 1 (b). The detailed circuit model of a single CNT is illustrated in Fig. 1 (c) and Fig. 1 (d) for a healthy CNT and for a damaged one, respectively. The circuit model is addressed to characterize the electrical damage effect of a CNT interruption by simulating the small signal behavior of the circuit of Fig. 2 (a) representing the local circuital model of single CNT interconnecting the drain and the source electrodes of a n-channel MOSFET transistor (see Fig. 1 (d)).

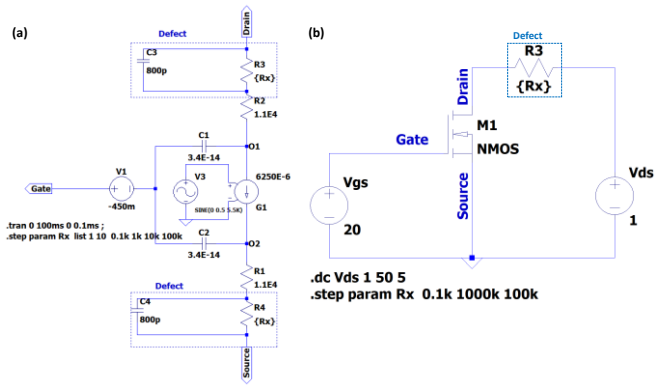


Figure 2. LTSpice circuit model: (a) CNT n-MOSFET layout slow-variation circuit including defect circuit model; (b) whole n-MOSFET model including the macroscopic effect of a damaged transistor.

The model of Fig. 2 (a) is extracted from the theoretical model discussed in [17]-[25], by adding the equivalent defect circuit where the main electrical contribution is provided by the resistance in series [18]. Specifically, the circuit of Fig. 2 (a) represents the model simulating locally the electrical variables characterizing the region between the source the drain and the gate port of the transistor. The main parameters of the circuit of Fig. 2 (a) are listed in Table I (parameters found in the state of the art).

TABLE I. CIRCUITAL ELEMENT OF THE LAYOUT OF FIG. 2 (A) [19],[21],[23].

| Circuit Parameter | Value |
|---|---|
| $R_1$, $R_2$ [Ω](low CNT density) | $1.1 \cdot 10^4$ |
| $C_1$,$C_2$ [F] (low CNT density) | $3.4 \cdot 10^{-14}$ |
| $G_1$ [S/μm] (*n*-type) | 6250 |
| $V_1$ [mV] (flat band) | -450 |
| $C_3$,$C_4$ [F] (parasitic capacitance) | $800 \cdot 10^{-12}$ |

### B. FEM Model

The proposed Two-Dimensional (2D) FEM model is adopted to understand the macroscopic effect of different CNTs damaged on the same surface. The damage is modelled by calculating the surface density current $J$ of a spatial domain modelling aligned CNTs linking source and drain pins. The FEM modelling is based on the setting of a 2D spatial domain enclosing the region between the source and the drain electrodes. The CNTs are modelled by thin rectangular boxes which are excited by a density of current $J$ (left boundary condition). The right side of the 2D spatial domain is the boundary condition able to absorb the electromagnetic field. The model is suitable to implement the percolation physical effect [11],[24],[26] characterizing the surface electrical current coupled by the nanostructures placed on the transistor surface thus facilitating the comprehension of the current flowing through links of aligned CNTs. An input $J$ of 1 A/m$^2$ is adopted as surface density flowing from the drain electrode to the source one (the electrodes are the left and the right contour of the boundaries of the spatial domain). The equation solved to estimate the current surface density $J$ is:

$$\nabla \cdot J = -(\partial \rho_v / \partial t) \tag{1}$$

, being $\rho_v$ the charge density. In Table II are listed the main physical and geometrical parameters adopted for the FEM simulation. The used FEM assumptions are enough to characterize a main cyber-physical model describing the electrical current discontinuity due to CNTs interruptions (damaged CNTs).

TABLE II. PARAMETERS USED FOR FEM SIMULATION.

| Parameter | Value |
|---|---|
| 2D Spatial domain | 280 μm x 160 μm |
| CNT length | 50 μm |
| Input $J$ ($Jx$ component) | 1 A/m$^2$ |
| CNT conductivity $\sigma_{CNT}$ | 3000 S/m |
| Substrate conductivity $\sigma_{SUB}$ (Silicon Carbide) | 1000 S/m |

## III. RESULTS

### A. LTSpice circuit results: electrical characterization of the CNTs breakage and sensitivity response

The parametric analysis is performed by means the LTSpice tool, a SPICE-based analog electronic circuit open-source simulator (Version x64: 24.1.8): the analysis is executed by changing the electrical resistance Rx modelling, together with the parasitic capacitances (C3 and C4), the surface defect due to the breaking of the CNTs (see Fig. 1 (d)). Specifically, the electrical resistance Rx indicates the main effect of the CNTs defects on the transistor surface. In order to simulate different damage effects of the whole area between the source and the drain regions, the Rx value is changed between 1 Ω and 100 kΩ with a step increase of 10 Ω by following a deterministic approach. This assumption is suitable for the sensitivity analysis of the voltage and current signals versus the defect extent. Figure 3 (a) and (b) show the time domain simulation of the circuit of Fig. 2 (a) calculating the $V_{drain}$ and $V_{source}$ signals. The performed simulation is useful to estimate the sensitivity response versus the Rx parameter (see Fig. 4): a low sensitivity of $V_{drain}$ signal is observed for Rx values between 10 Ω and 1 kΩ. The same sensitivity is checked also for the $V_{source}$ signal.

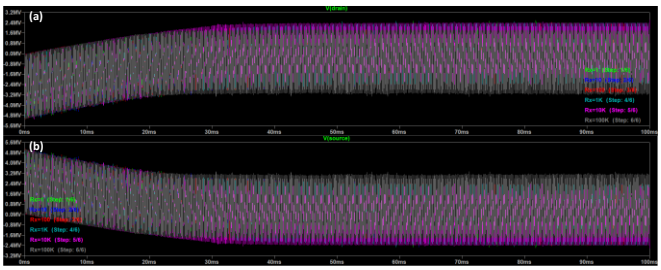


Figure 3. (a) voltage $V_{drain}$ and (b) $V_{source}$ signals versus the time varying the parameter Rx modelling defect effect. The indicated voltage scale is in mV.

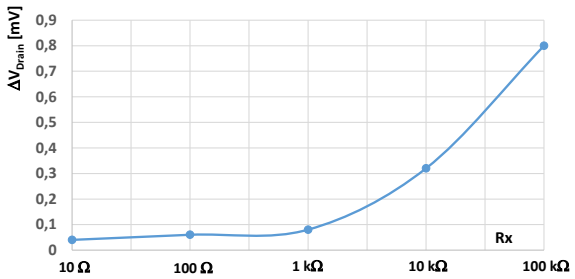


Figure 4. $V_{drain}$ sensitivity response. The variation $V_{drain}$ of the voltage signal is calculated by considering Rx = 1Ω as reference value (gap compared to the reference value).

The circuit model of Fig. 2 (b) is suitable to understand the global effect of the CNT defects in an n-MOSFET integrated circuit. The Rx parameter is connected directly at the drain link to estimate the sensitivity of the drain current signal ($I_d$) by considering a DC simulation. In Fig. 5 is illustrated a simulation of the $I_d$ signal versus the $V_{ds}$ voltage indicating a decrease of the $I_d$ current trend with an increase of the Rx resistance.

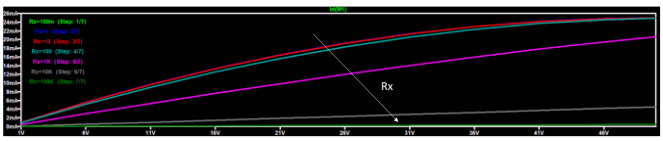


Figure 5. Drain current of the circuit of Fig. 2 (b) versus the $V_{ds}$ voltage. The parametric LTSpice simulation is performed changing the defect parameter Rx.

The macroscopic effect of the sensitivity response versus defects is shown in Fig. 6 estimating the variation of the drain current ($\Delta I_d$) by comparing a circuit with Rx null and fixing $V_{ds}$ = 50 V and $V_{gs}$ = 50 V. A significant variation of the current signal is checked for Rx values greater than 100 Ω. The sensitivity responses highligths a nonlinear trend of the of the electrical current $I_{drain}$ and of the voltage $V_{drain}$ (see Fig. 4 and Fig. 6) versus the Rx parameter. At macroscopic scale the density of current associated to a group of CNTs is provided by:

$$J_z(z,\omega) = \sigma(\omega)\, E_z(z,\omega) \qquad (2)$$

being $\sigma$ the conductivity typically characterized by a nonlinear behavior.

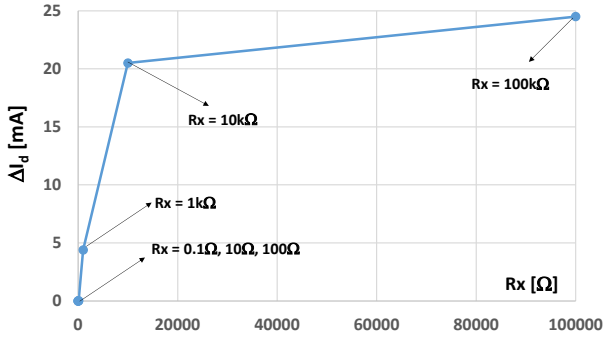


Figure 6. Sensitivity response of $I_{drain}$ current ($I_d$) versus the Rx parameter.

## B. FEM Results

Figures 7 (a),(b),(c) and (d) illustrate the effect of the aligned CNTs interruptions about the coupled density of current flowing from an electrode to the other one. As expected, the best condition about electrical current coupling is checked for the perfectly aligned CNTs (higher $J$ intensity). In Table II are listed the main physical and geometrical parameters adopted in the FEM simulation. The simulations of Fig. 7 are performed by considering two calculus lines: the first (calculus line 1) is a cross section linking all aligned and parallel CNTs (parallel to the source and drain electrodes), and the second one (calculus line 2) is a longitudinal section corresponding to a pattern of a single CNT line (line orthogonal to the two electrodes source and drain).

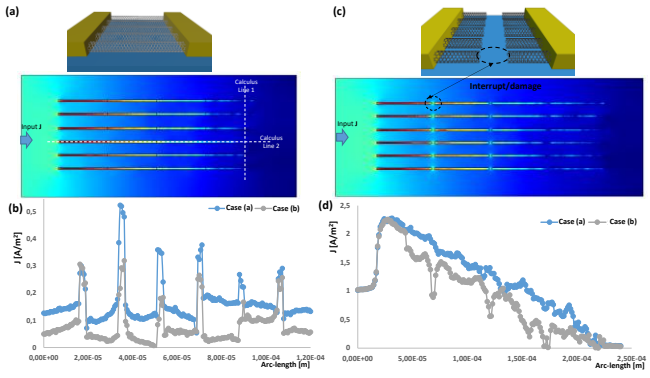


Figure 7. (a) $J$ distribution on a surface containing aligned CNTs. (b) $J$ distribution along the calculus line 1 (arch-length coinciding with a cross section) for both the configurations (case (a) perfectly aligned and case (b) of the interrupted case). (c) $J$ distribution on a surface containing aligned and detached CNTs (theoretical modelling of damaged/interrupted CNTs). (d) $J$ distribution along the calculus line 2 (arch-lengrth coinciding with the longitudinal section crossing an aligned CNTs array) for both the configurations (case (a) perfectly aligned and case (b) of the interrupted case).

## IV. HEALING AND SELF-HEALING CONTROL PROCEDURES AND DISCUSSION

### *A. Protocol to control self-healing process*

Self-healing process of aligned CNTs devices can be achieved by adopting specific substrates such as elastomer composite films: the self-healing film can be healed applying a voltage of 1.18 V/mm by through the electro-thermal effect of aligned CNTs or by adopting a light source [15]. The self-healing of the film is due to the electrical reconnection of CNTs through the transesterification-induced process (process of exchanging the organic functional group of an ester with the organic group of an alcohol) [15]. Alternatively, an automatic healing process can be enabled by CNTs spray deposition [16]: after a reading of variation of voltage or current characteristics of the transistor, CNTs could be deposited locally in the region between source and drain electrodes thus restoring the initial transistor working conditions (initial I-V characteristics). In Fig. 8 (a) and Fig. 8 (b) are sketched both the mentioned approaches.

The controlled healing and the self-healing process can be optimized by the following procedure mapped in the workflow of Fig. 9:

a) Step 1 (restoration of the experimental setup): the working condition of the experimental setup must be the same of the first experimental setup adopted to characterize the transistor (same room temperature, light conditions, same electrical and mechanical setting of the probe station or multimeter, etc.);

b) Step 2 (transistor I-V measurements): I-V characteristics are achieved by performing measurements in stable setup conditions and by repeating measurements observing stable values (it is preferable to acquire at least five different measurements by estimating the arithmetic average);

c) Step 3 (tolerance check): if the average measure is within the accepted tolerance by comparing sensitivity responses (as Fig. 4 and Fig. 6) then it is only planned the healing process by tracking and comparing the new measures with previous ones (step 4(a)), otherwise (total degradation case) it is triggered the healing process restoring the efficiency of the nanostructures connecting source and drain electrodes (step 4(b));

d) Step 5 (new transistor I-V measurements): the measurements are repeated after the healing process according with the conditions of step (1);

e) Step 6 (second step of the tolerance check): if the average measure is within the accepted tolerance, it is only updated the sensitivity response (possibly changed after the healing restoring the device efficiency), otherwise it is enabled again the healing process and are executed again the I-V measurements (return to the step (5));

f) Step 7 (tolerance update): after the step 4 (b) must be updated, if necessary, the sensitivity responses due to the nano structured morphological change of the transistor surface;

g) Step 8: update of the healing plan.

The listed point refers to a new protocol named "*TC34_STR1_1_HEAL_R1(2026): transistor healing and I-V measurements*". The protocol is related to the measurement of the I-V characteristics of a transistor to be healed after a degradation of its responses. Figure 9 summarizes all the steps of the protocol by means the standard Business Process Modelling and Notation (BPMN) modelling (ISO/IEC 19510:2013, Information technology, Object Management Group Business Process Model and Notation) typically adopted for industrial applications [27], and used for measurement protocols [28]. We observe that the protocol of Fig. 9 is related to a generic healing process of a transistor constituted by nanostructures and is subject to changes/revisions in accordance with further validations of the TC 34.

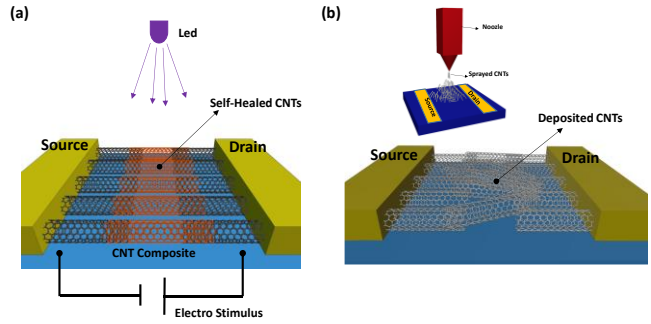


Figure 8. (a) CNTs sealf-healing and electro-thermal effect. (b) Automatic healing proccess controlled automatically by a nozzle (spray deposition).

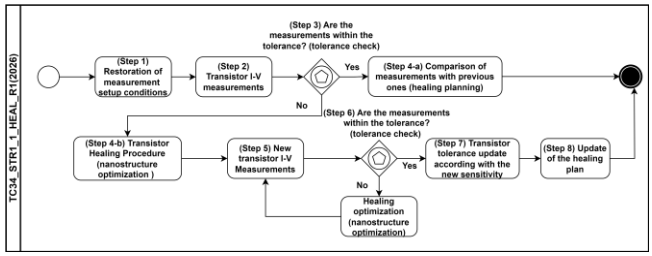


Figure 9. BPMN workflow implementing the guidelines of the I-V measurement protocol: "*TC34_STR1_1_HEAL_R1(2026): transistor healing and I-V measurements*".

We observe that the healing process should be activated gradually allowing the possibility to optimize the transistor efficiency into different successive steps (a drastically increase of CNTs deposition could change drastically the I-V characteristics) thus supporting the characterization of the sensitivity responses (also verifying for example thermostability conditions). Furthermore, the process to control externally the stimuli for the healing process should be before tested and validated. In this direction a preventive simulation or the adoption of Artificial Intelligence (AI) algorithms [11] could facilitate the improvement of the self-healing or the in general the healing process.

### B. Digital Twin (DT) model and discussions

The combined use of circuit simulation and FEM tools, consitituting the Digital Twin (DT) model, could improve the design of the small decices and circuits [29]-[34] and, according with the research proposed in this paper, predict the elecrtrical behavior of a damaged micro-device. Specifically, the SPICE circuit provides results regarding the sensitivity of the variation of the equivalent circuit parameters, while the FEM analysis supports the understanding of what happens macroscopically from a physical point of view. The combined use of both tools allows to improve the representation of the complete cyber-physical scenario supporting the experimental analysis discussed in the protocol of Fig. 9. The integration of AI into DT models is still to be explored, but it could be useful for predicting transistor responses under real-scenario or noisy conditions, allowing possible signal correction. The DT could be scaled to other devices and sensors with large areas of CNTs and enhancing electrical current. The combined use of circuit and FEM simulations is suitable to characterize CNTs damaged on the external surface area between source and drain electrodes. This area can be localized by means of a microscope which could automate a periodical image check of the CNTs status also using AI defect classification. The processed images can be associated with the measurements of the steps 2 and 5 of Fig. 9 to calibrate the healing process and to check the progressive CNTs deteriorations characterizing at the same time the related I-V characteristic (deterministic approach). Furthermore, the use of the FEM simulation allows to study locally the damage efffect by considering also the single CNT (simulation of the real damage, due to a structural defect or localized imperfections, different from the ideal case of a regular cut as shown in Fig. 7). The input normalized $J$ value of 1 A/m$^2$ can be changed as a variable parameter controlling the electrical current flux of the transistor surface and modelling the different behavior of the device changing the input power. Other possible improvements of the circuit model can be performed by setting the Rx value with a nonlinear trend following the real physcal behavior of the surface conductivity. Furthermore, the percolation effect allows to better comprehend the dynamical behavior of the total surface resistance changing the Rx values. The Rx change is an indicator of the transitor efficiency sensing at the same time the CNTs healty.

## V. Conclusion

The proposed model introduces an innovative approach to characterize CNTs based n-channel MOSFET transistors for healing processes of generic nanostructured transistors in modern electronics. The SPICE-based circuit is adopted to characterize the sensitivity responses of the damaged transistors by characterizing locally and macroscopically the variation of the electronic signals due to defects modelled by variable circuital resistances. The FEM approach is then applied to facilitate the comprehension of the effect of the possible damaged CNTs embedded in transistor devices proving the degradation of the electrical signal after the interruptions of CNTs links. Finally, the study is addressed on the formulation of guidelines for measurements of I-V performance of a generic healed transistor made by nanostructures. The paper's study is preliminary about the physical aspects involving CNTs damage characterization. Future work will be addressed on the model validation by means experimental data and accurate numerical benchmarking by focusing the attention on industrial sensing applications and damage classification.


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